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EXAMINER	
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2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/727,602	TANAKA ET AL.	
	Examiner	Art Unit	
	Chun-Kuan (Mike) Lee	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 February 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,9-11 and 13-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,9-11 and 13-15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO ARGUMENTS

1. Applicant's arguments filed 02/28/2007 have been fully considered but they are not persuasive. The rejection of claims 5 and 8 under 35 U.S.C. 112 second paragraph are withdrawn. Currently, claims 2-3, 5-8, 12 and 16-18 are canceled and claims 1, 4, 9-11 and 13-15 are pending for examination.

2. In response to applicant's arguments, on page 8, regarding independent claim 1 rejected under 35 U.S.C. 103(a) that the combination of references do not show the claimed process of deactivating the failed machine, and after the failed machine is deactivated, the system is recovered by switching the control of I/O device to the secondary computer; applicant's arguments have fully been considered, but are not found to be persuasive.

Please note that in accordance to MPEP 2113, it is stated that:

"Even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. The patentability of a product does not depend on its method of production. If the product in the product-by-process claim is the same as or obvious from a product of the prior art, the claim is unpatentable even though the prior product was made by a different process."

The final product associated with the claimed invention is the recovering of the system as the failed machine is detected and deactivated, and then the standby virtual

machine would establish connection with the I/O device and become activated. Since it appears that neither the Specification nor the Drawings disclose any advantages to have the failed virtual machine be deactivated following the detection of error and before the switching of the connection to the I/O device. Therefore, in accordance with the MPEP 2113, the goal achieve by the claimed process would have been obvious from the prior art references. More specifically, Stiffler's teaching achieves the same goal of system recovery, except the deactivation of the failed virtual machine is after the standby virtual machine establishing connection with the I/O device and become activated.

As the applicant applied the same arguments as presented for independent claim 1 towards independent claims 9 and 13, the examiner also applies the same response, as discussed in detail above, towards independent claims 9-13.

I. INFORMATION CONCERNING OATH/DECLARATION

Oath/Declaration

3. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in **37 C.F.R. 1.63.**

II. INFORMATION CONCERNING DRAWINGS

Drawings

4. The applicant's drawings submitted are acceptable for examination purposes.

III. REJECTIONS BASED ON 35 U.S.C. 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 1, 4, 10-11, 13 and 15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

6. As per claims 1 and 13, in regards to the claimed limitation "a control signal received from said selected virtual machine," it appears unclear how "said selected virtual machine" provides the "control signal," because it seems "said selected virtual machine" is the LPAR0 of Figure 10 in the Drawings and the "control signal" is associated with the "deactivate COMMAND" of Figure 10 in the Drawings. Therefore it appears that it is the standby LPAR (i.e. LPAR1) that is providing the control signal. The examiner will assume the following claimed limitation "a control signal received from a standby virtual machine" for the current examination.

7. As per claims 4, 11 and 15, in regards to the claimed limitation "said first virtual machine sends to said control program a command to switch a state of logical connection to said I/O device, said first virtual machine sends to said control program a

command to deactivate or activate virtual machines said second virtual machine, said control program capable of deactivating or activating a virtual machine with respect to said control program in response to said command being received," it appears that "said first virtual machine" is the LPAR0 of Figure 10 in the Drawings and "said second virtual machine" is the LPAR1 of Figure 10 in the Drawings, therefore it appears unclear how the first virtual machine (LPAR0) is sending the command (i.e. "deactivate COMMAND" of Figure 10) for deactivation or activation of the second virtual machine (LPAR1) for implementing the switching, as such command is send by the second virtual machine (LPAR1).

8. As per claim 10, it appears unclear as to how "said first virtual machine" (LPAR0 of Figure 10) is sending the "control signal" (deactivate COMMAND" of Figure 10) as it appears that the "control signal" is send by the LPAR1 (standby computer) of Figure 10.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

9. Claims 1, 4, 9-11, 13 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said virtual machine" in claim 1, lines 17-18. There is insufficient antecedent basis for this limitation in the claim.

Claim 9 recites the limitation "said virtual machine" in claim 9, lines 11-12. There is insufficient antecedent basis for this limitation in the claim.

Claim 10 recites the limitations "said first virtual machine," "said second virtual machine" and "said port" in claim 10, lines 4-7. There is insufficient antecedent basis for this limitation in the claim.

Claim 11 recites the limitations "said first virtual machine," "said second virtual machine" and "said control program" in claim 11. There is insufficient antecedent basis for this limitation in the claim.

Claim 13 recites the limitation "said virtual machine" in claim 13, lines 12-13. There is insufficient antecedent basis for this limitation in the claim.

10. As per claims 1 and 13, it appears unclear as to which "virtual machine" the applicant is referring to. The examiner will assume the following claimed limitation "said selected virtual machine" for the current examination.

11. As per claim 4, it appears unclear as to which "said command" the applicant is referring to. In combination with the rejection of claim 4 under 35 U.S.C. 112 first paragraph as discussed in detail above, the examiner will assume the following claimed limitation "wherein said second virtual machine sends to said control program a command to switch a state of logical connection to said I/O device, said second virtual machine sends to said control program said command to deactivate or activate said first virtual machine, said control program deactivating and activating said first virtual

machine with respect to said control program in response to said command being received," for the current examination.

12. As per claim 9, it appears unclear as to which "said virtual machine" and virtual machine" the applicant is referring to. The examiner will assume the following claimed limitation "wherein in response to detection of occurrence of an error in a first computer, said first computer is deactivated, then connection to said I/O device is switched to a standby computer, said standby computer is set as an active computer, and said deactivated first computer is repaired and set as a standby computer" for the current examination.

13. As per claim 10, it appears unclear as to which "said first virtual machine," "said second virtual machine" and "said port" the applicant is referring to. In combination with the rejection of claim 10 under 35 U.S.C. 112 first paragraph as discussed in detail above, the examiner will assume the following claimed limitation "wherein said signal generating means sends the interruption signal to said second computer to change said state of logical connection of said single port to said first computer according to a control signal received from said second computer" for the current examination.

14. As per claim 11, it appears unclear as to which "said first virtual machine," "said second virtual machine," "said control program," "said command" and said interruption signal the applicant is referring to. In combination with the rejection of claim 11 under 35

U.S.C. 112 first paragraph as discussed in detail above, the examiner will assume the following claimed limitation "wherein said second computer sends to a control program a command to switch a state of logical connection to said I/O device, said second computer sends to said control program said command to deactivate or activate said first computer, said control program deactivating and activating said first computer with respect to said control program in response to said command being received;

wherein said control program includes a PCI connection allocating table, said PCI connection allocating table is changed so that connection with I/O device is switched to said second computer according to a control signal received, in response to said PCI connection allocating table being changed, said control program generates said interruption signal, and in response to said interruption signal being received by said second computer, said second computer changes connection to said I/O device, and

wherein said first computer is rebooted to reconstruct said first computer as a standby machine and a CPU allocation rate of said first computer is set to be low," for the current examination.

15. As per claim 15, it appears unclear as to which "said command" the applicant is referring to. In combination with the rejection of claim 4 under 35 U.S.C. 112 first paragraph as discussed in detail above, the examiner will assume the following claimed limitation "wherein said second virtual machine sends to said control program a command to switch a state of logical connection to said I/O device, said second virtual

machine sends to said control program said command to deactivate or activate said first virtual machine, said control program deactivating and activating said first virtual machine with respect to said control program in response to said command being received," for the current examination.

IV. ALLOWABLE SUBJECT MATTER

Allowable Subject Matter

16. Claims 4, 11 and 15 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 1st and 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

V. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

17. Claims 1 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of Pittelkow et al. (US Patent 7,003,688).

18. As per claim 1, Stiffler teaches a computer system, comprising:

a plurality of virtual machines (primary computer 601 and secondary computer 603 of Fig. 6) formed on a control program of a computer (Fig. 6), wherein the primary and the secondary computer are physical partition of the computer system and is implemented in the virtual environment;

an I/O device (Fig. 6, ref. 616) connected to a PCI bus (Fig. 6, ref. 610, 624) of said computer and shared among said plurality of virtual machines (physical partitioned computers) (col. 9, l. 52 to col. 10, l. 10);

a port disposed in said I/O device and connected to said PCI bus (col. 9, ll. 52-56 and col. 10, ll. 3-7), wherein the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the I/O device would obviously have the single port; and

a PCI connection allocating means for setting a state of logical connection between selected one of said plurality of virtual machines (e.g. physical partitioned computers including primary computer 601 and secondary computer 603 of Fig. 6) and said port(Fig. 9 and col. 10, ll. 20-64); and

I/O device switching means for updating said state of connection set by said PCI connection allocating means according to a control signal received from a standby virtual machine (e.g. physical partitioned computer including the secondary computer) (Fig. 9 and col. 10, ll. 20-64), wherein the secondary computer implement the takeover control signal procedure,

wherein said selected virtual machine (e.g. physical partitioned computer having the primary computer) changes its state of logical connection to said I/O device (e.g.

disk array) according to the setting by said PCI connection allocating means (Fig. 6; Fig. 9 and col. 10, ll. 20-64), wherein the state of logical connection between the secondary computer and the disk array is changed by becoming active resulted form the takeover procedure, and the state of logical connection between the primary secondary and the disk array is deactivated as the primary computer is taken off-line,

wherein in response to detection of occurrence of an error (e.g. in a fault state) in said selected virtual machine (e.g. primary computer), said selected virtual machine is deactivated, the connection to said I/O device then switches to said standby virtual machine (e.g. secondary computer), said standby virtual machine is set as an active virtual machine, said deactivated virtual machine (e.g. primary computer) is repaired and set as a standby virtual machine (col. 10, ll. 20-64 and col. 14, ll. 35-63).

Stiffler does not expressly teach a computer system comprising:

wherein the port is a single port;

wherein the PCI connection allocating means for setting a state of logical connection between selected at most one of said plurality of physical partitioned computers and said port at a time; and

wherein the deactivation of the error detected virtual machine occurs before the I/O device switching the connection to the standby virtual machine.

Pittelkow teaches a system and method comprising

a storage assembly (Fig. 6, ref. 612) connected to a switch (Fig. 6, ref. 608) through a controller (Fig. 6, ref. 610), wherein a plurality of servers (Fig. 6, ref. 602, 604, 606) is coupled to the storage assembly through the switch, wherein said switch and

controller enable at most one of said plurality of servers to be connected to the storage assembly at a time (col. 18, ll. 20-56); and

a configuration and control board for providing notification of failures (col. 8, ll. 49-52).

Stiffler and Pittelkow are analogous art because they are from the same field of endeavor as they are both associated with the connection of a plurality of computer to a storage peripheral device.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Pittelkow's switch and controller into Stiffler's computer system. The resulting combination of the references further teach:

said I/O device having the single port and is connected to said PCI bus, because the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the primary computer echoed by the second computer, therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer;

having at most the secondary computer connected to the disk array at a time as the primary computer is taken off-line; and

wherein it would have been obvious to implement the deactivation of the error detected virtual machine before the I/O device switching the connection to the standby virtual machine.

The suggestion/motivation for doing so would have been for the benefit of increase the robustness of the interconnection between the disk array and the plurality

of computer, because if one of the interconnection were to fail, another interconnection can be established (Pittelkow, col. 18, ll. 41-56).

Therefore, it would have been obvious to combine Pittelkow with Stiffler for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established to obtain the invention as specified in claim 1.

19. As per claims 13, Stiffler teaches a method for sharing an I/O device (disk array 616 of Fig. 6) connected to a PCI bus (Fig. 6, ref. 610, 624) of a computer among a plurality of virtual machines (Fig. 6, ref. 601, 603) formed on a control program of said computer, comprising the steps of:

enabling said I/O device to set a state of logical connection between said selected virtual machine (primary computer 601 of Fig. 6) (Fig. 6; Fig. 9 and col. 10, ll. 20-64) and a port of said I/O device connected to said PCI bus (Fig. 6, ref. 610, 624) through said port (col. 9, l. 52 to col. 10, l. 10), wherein the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer therefore the disk array would obviously have the single port

changing said state of logical connection between said port and said selected virtual machine (e.g. primary computer) according to a control signal received from a standby virtual machine (e.g. secondary computer) (Fig. 9 and col. 10, ll. 20-64), wherein upon implementing the takeover control signal procedure by the secondary computer, the logical connection between the primary computer and the disk array

become deactivated as the primary computer is take off-line, and the logical connection between the disk array and the secondary computer becomes active and the secondary computer becomes the new primary computer; and

in response to detection of occurrence of an error (e.g. in a fault state) in said selected virtual machine (e.g. primary computer), deactivating said selected virtual machine; switching connection to said I/O device to said standby virtual machine (e.g. secondary computer); setting said standby virtual machine as an active virtual machine; and repairing deactivated virtual machine, and setting the repaired deactivated virtual machine as a standby virtual machine, wherein said computer includes first (e.g. primary computer) and second (e.g. secondary computer) virtual machines formed therein (col. 10, ll. 20-64 and col. 14, ll. 35-63).

Stiffler does not expressly teach the method comprising:

wherein the port is a single port;

selecting at most one virtual machine among said plurality of virtual machines at a time; and

wherein the deactivation of the error detected virtual machine occurs before the I/O device switching the connection to the standby virtual machine.

Pittelkow teaches a system and method comprising

a storage assembly (Fig. 6, ref. 612) connected to a switch (Fig. 6, ref. 608) through a controller (Fig. 6, ref. 610), wherein a plurality of servers (Fig. 6, ref. 602, 604, 606) is coupled to the storage assembly through the switch, wherein said switch and

controller enable at most one of said plurality of servers to be connected to the storage assembly at a time (col. 18, ll. 20-56).

Stiffler and Pittelkow are analogous art because they are from the same field of endeavor as they are both associated with the connection of a plurality of computer to a storage peripheral device.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Pittelkow's switch and controller into Stiffler's computer system. The resulting combination of the references further teach:

the I/O device's connection to the PCI bus utilizes the single port, because the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer, therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer;

having at most the secondary computer connected to the disk array at a time as the primary computer is taken off-line; and

wherein it would have been obvious to implement the deactivation of the error detected virtual machine before the I/O device switching the connection to the standby virtual machine.

The suggestion/motivation for doing so would have been for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established (Pittelkow, col. 18, ll. 41-56).

Therefore, it would have been obvious to combine Pittelkow with Stiffler for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established to obtain the invention as specified in claim 13.

20. Claims 9-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of Pittelkow et al. (US Patent 7,003,688) and "Computer Input/Output"

21. As per claim 9, Stiffler teaches an I/O device (disk array 616 of Fig. 6) connected to a PCI bus of a computer (primary computer 601 and secondary computer 603 of Fig. 6), comprising:

a port connected to said PCI bus (Fig. 6 and col. 10, ll. 20-64), wherein the disk array is duplicated by having all disk stored initiated on the primary computer echoed by the second computer;

an operating system performing hot-add/remove an I/O device (disk array 616 of Fig. 6) (col. 14, ll. 54-58), wherein the hot-add/remove the I/O device is implemented as all user tasks continue to be executed with no lost of data or program continuity;

change the state of logical connection of said port according to a control signal received from said computer (Fig. 6 and col. 10, ll. 20-64), wherein when the secondary computer detect error with the primary computer, the secondary computer implement

the takeover control signal procedure to change the state of logical connection between the primary computer and the disk array by having the primary computer taken off-line;

wherein said computer changes its state of logical connection to said port (Fig. 6 and col. 10, ll. 20-64), wherein upon the secondary computer implementing the takeover control signal procedure, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer; and

wherein in response to detection of occurrence of an error (e.g. in a fault state) in a first computer (e.g. primary computer), said first computer is deactivated, connection to said I/O device is switched to a standby computer (e.g. secondary computer), said standby computer is set as an active computer, and said deactivated first computer (e.g. primary computer) is repaired and set as a standby computer (col. 10, ll. 20-64 and col. 14, ll. 35-63).

Stiffler does not expressly teach the I/O device connected to the PCI bus of the computer, comprising:

wherein the port is a single port;

signal generating means for generating an interruption signal used to change the state of logical connection of said port according to a control signal received from said computer;

the interrupt signal causes the hot-add/remove of the I/O device; and

when receiving said interruption signal said computer changes its state of logical connection to said port; and

wherein the deactivation of the error detected first computer occurs before the I/O device switching the connection to the standby computer.

Pittelkow teaches a system and method comprising

a storage assembly (Fig. 6, ref. 612) connected to a switch (Fig. 6, ref. 608) through a controller (Fig. 6, ref. 610), wherein a plurality of servers (Fig. 6, ref. 602, 604, 606) is coupled to the storage assembly through the switch, wherein said switch and controller enable at most one of said plurality of servers to be connected to the storage assembly at a time (col. 18, ll. 20-56); and

a configuration and control board for providing notification of failures (col. 8, ll. 49-52).

Stiffler and Pittelkow are analogous art because they are from the same field of endeavor as they are both associated with the connection of a plurality of computer to a storage peripheral device.

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Pittelkow's switch, controller and the notification of failure into Stiffler's computer system. The resulting combination of the references further teach:

said I/O device having the single port and is connected to said PCI bus, because the disk array (i.e. I/O device) is duplicated by having all disk stored initiated on the

primary computer echoed by the second computer, therefore the disk array would obviously have the single port, which may be connected to a communication network to be accessible by both the primary computer and the secondary computer; and

wherein it would have been obvious to implement the deactivation of the error detected first computer before the I/O device switching the connection to the standby computer.

The suggestion/motivation for doing so would have been for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established (Pittelkow, col. 18, ll. 41-56).

Therefore, it would have been obvious to combine Pittelkow with Stiffler for the benefit of increase the robustness of the interconnection between the disk array and the plurality of computer, because if one of the interconnection were to fail, another interconnection can be established to obtain the invention as specified in claim 9.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler and Pittelkow's computer system. The resulting combination of the references teaches further comprising:

generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer; and

the disk array (i.e. I/O device) is hot-removed from the primary computer in response to the primary computer receiving and running the interrupt signal.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler and Pittelkow because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

22. As per claim 10, Stiffler, Pittelkow and "Computer Input/Output" teach all the limitations of claim 9 as discussed above, where Stiffler and "Computer Input/Output" further teach that the system comprising:

wherein said signal generating means sends the interruption signal to said second computer (e.g. secondary computer) to change said state of logical connection of said single port to said first computer (e.g. primary computer) according to a control signal received from said second computer (Stiffler, Fig. 6 and col. 10, ll. 20-64 and "Computer Input/Output", section 4), wherein upon the disk array receiving the takeover control signal procedure from secondary computer, the interrupt is generated to inform the second computer for becoming active and operating as the new primary computer.

23. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stiffler et al. (US Patent 6,622,263) in view of Pittelkow et al. (US Patent 7,003,688) as applied to claim 13 above, and further in view of "Computer Input/Output".

Stiffler and Pittelkow teach all the limitations of claim 13 as discussed above, where Stiffler further teaches the system comprising wherein said step of changing said state of logical connection includes a step of changing said state of logical connection between said port and said selected virtual machine (Fig. 6 and col. 10, ll. 20-64), wherein the state of logical connection between the primary computer and the disk array is deactivated and the state of logical connection between the secondary computer and the disk array is activated.

Stiffler and Pittelkow does not teach the system comprising:

generating an interruption to notify said selected virtual machine of a change of said state of logical connection of said I/O device; and

a step of enabling said selected virtual machine that receives said interruption to change said state of logical connection to said I/O device according to said setting of said state of logical connection.

"Computer Input/Output" teaches the Interrupt Driven I/O (Section 4), wherein the sequence of events is as follows:

the I/O module (I/O device) interrupts the CPU;

the CPU (computer) finishes executing the current instruction;

the CPU acknowledges the interrupt;

the CPU saves its current state; and

the CPU jumps to a sequence of instructions which will handle the interrupt (Section 4).

It would have been obvious to one of ordinary skill in this art, at the time of invention was made to include Computer Input/Output's interrupt signal into Stiffler and Pittelkow's computer system. The resulting combination of the references teaches further comprising generation of the interrupt signal by the disk array when the disk array receives the takeover control signal procedure from the secondary computer and when the primary and secondary computers receive the disk array's interrupt, the state of logical connection between the primary computer and the disk array is deactivated as the primary computer will be taken off-line and the state of logical connection between

the secondary computer and the disk array is activated as the secondary computer takes over to commence operating as the new primary computer.

Therefore, it would have been obvious to combine Computer Input/Output with Stiffler and Pittelkow because not only is the utilization of interrupt signals within the computer system well known, this also provide the benefit of the CPU not to continually poll input devices to see if it must read any data.

VI. CLOSING COMMENTS

Conclusion

a. STATUS OF CLAIMS IN THE APPLICATION

The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**:

a(1) CLAIMS REJECTED IN THE APPLICATION

Per the instant office action, claims 1, 4, 9-11 and 13-15 have received a final action on the merits. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

b. DIRECTION OF FUTURE CORRESPONDENCES

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun-Kuan (Mike) Lee whose telephone number is (571) 272-0671. The examiner can normally be reached on 8AM to 5PM.

IMPORTANT NOTE

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

May 04, 2007

Chun-Kuan (Mike) Lee
Examiner
Art Unit 2181

DONALD SPARKS
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